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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/780,586	02/19/2004	Takashi Takamura	118394	2499

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EXAMINER	
GEBREMARIAM, SAMUEL A	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 02/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/780,586	TAKAMURA, TAKASHI	
	Examiner	Art Unit	
	Samuel A. Gebremariam	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 5 and 6 are objected to because of the following informalities: The limitation of an "image device" as recited in claim 5 and 6 appears to be a typographical error. Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> **A person shall be entitled to a patent unless –**
>
> **(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.**

3. Claims 1-6 are rejected under 35 U.S.C. 102(b) as being anticipated by Miida, US patent No. 6,051,857.

Regarding claim 1, Miida teaches (figs. 2-7B) a solid-state imaging device, comprising: a pixel array having a plurality of unit pixels (col. 3, lines 59-65 and refer to fig. 7A), each unit pixel including a photo diode (111) and an insulated gate field effect transistor (112) that detects a photocharge (fig. 3); and a control circuit (refer to fig. 7A) that controls the operation of the pixel array, wherein: the photo diode (111) and the insulated gate field effect transistor (112) share a well region (15) of a first conductivity type (p) that is formed in a semiconductor layer (12) of a second conductivity type (n), the semiconductor layer of the second conductivity type formed on a semiconductor substrate (11) of the first conductivity type (p); the insulated gate field effect transistor

comprising: a source diffused region (16) of the second conductivity type (n) formed on a surface of the well region (15); a drain diffused region (17a) of the second conductivity type (n) formed on a surface of the semiconductor layer (12) other than the surface of the well region (portion of 17a is formed on the surface of the semiconductor layer 12 other than the surface of the well region 15); a gate electrode (19) formed over the well region between the drain diffused region (17a) and the source diffused region (16) with a gate insulating film (18) therebetween; a channel region (col. 9, lines 18-20) formed in the surface of the well region under the gate electrode and having an impurity layer of the second conductivity type (n); and a heavily doped buried layer (25) of the first conductivity type formed under the channel region in the well region and near the source diffused region (16), having an impurity concentration higher than that of the well region, and being an accumulation region that accumulates a charge of a given conductivity type generated in response to light incident on the photo diode (col. 9, lines 34-40).

The limitation of "the control circuit that applies predetermined voltage to the source diffused region and the gate electrode, respectively, by which the channel region is brought into a conductive state, so as to bias a junction region formed of the semiconductor substrate and the semiconductor layer in a forward direction, and the control circuit accumulates a predetermined amount of the charge of a predetermined conductivity type in the accumulation region thereby, and thereafter, discharges the charge of a predetermined conductivity type accumulated in the accumulation region" is not given patentable weight because it is considered an operational limitation.

While features of an apparatus may be recited either structurally or functionally, claims directed to an apparatus must be distinguished from the prior art in terms of structure rather than function. >In re Schreiber, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997) (The absence of a disclosure in a prior art reference relating to function did not defeat the Board's finding of anticipation of claimed apparatus because the limitations at issue were found to be inherent in the prior art reference); see also In re Swinehart, 439 F.2d 210, 212-13, 169 USPQ 226, 228-29 (CCPA 1971);< In re Danly, 263 F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959). "[A]pparatus claims cover what a device is, not what a device does." Hewlett-Packard Co. v. Bausch & Lomb Inc., 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990) (emphasis in original).

Regarding claim 2, Miida teaches the entire claimed structure of claim 1 above including a maximum amount of available charge of the predetermined conductivity type is accumulated in the accumulation region (col. 9, lines 34-40).

Regarding claim 3, Miida teaches the entire claimed structure of claim 1 above including the charge of the predetermined conductivity type being a hole when the first conductivity type is a P type and the second conductivity type is an N type (col. 9, lines 34-40).

Regarding claim 4, Miida teaches the entire claimed structure of claim 1 above including the charge of the predetermined conductivity type being an electron when the first conductivity type is an N type and the second conductivity type is a P type (col. 4, lines 39-58).

Regarding claim 5, Miida teaches (figs. 2-7B) a photodiode (111) disposed in a well region (15) of a first conductivity type (p) that is disposed on a semiconductor layer (12) of a second conductivity type (n) that is further disposed on a semiconductor substrate (11) of the first conductivity type (p); an insulated gate field effect transistor (112) that shares the well region with the photodiode, further comprising: a source diffused region (16) of the second conductivity type (n) disposed on a surface of the well region; a drain diffused region (17a) of the second conductivity type disposed on a surface of the semiconductor layer other than the surface of the well region (portion of 17a is formed on the surface of the semiconductor layer 12 other than the surface of the well region 15); a gate electrode (19) formed above the well region between the drain diffused region and the source diffused region with a gate insulating film (18) therebetween; a channel region (col. 9, lines 18-20) disposed in the surface of the well region under the gate electrode having an impurity layer of the second conductivity type (n); an accumulation region (25) that is heavily doped of the first conductivity type (p+), and that is disposed beneath the channel region and adjacent to the source diffused region (16 and refer to fig. 3), the accumulation region having an impurity concentration higher than that of the well region (refer to fig. 3) and that accumulates a charge of a given conductivity type generated in response to light incident on the photodiode.

The limitation of "a control circuit that during an accumulation period applies first predetermined voltages to the source diffused region and the gate electrode to cause the charge to accumulate in the accumulation region, and during a reading out period applies second predetermined voltages to the source diffused region and the gate

electrode to discharge the charge in the accumulation region" " is not given patentable weight because it is considered an operational limitation.

While features of an apparatus may be recited either structurally or functionally, claims directed to an apparatus must be distinguished from the prior art in terms of structure rather than function. >In re Schreiber, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997) (The absence of a disclosure in a prior art reference relating to function did not defeat the Board's finding of anticipation of claimed apparatus because the limitations at issue were found to be inherent in the prior art reference); see also In re Swinehart, 439 F.2d 210, 212-13, 169 USPQ 226, 228-29 (CCPA 1971);< In re Danly, 263 F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959). "[A]pparatus claims cover what a device is, not what a device does." Hewlett-Packard Co. v. Bausch & Lomb Inc., 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990) (emphasis in original).

Regarding claim 6, Miida teaches an image device, comprising: a photodiode (111) disposed in a well region (15) of a first conductivity type that is disposed on a semiconductor layer (12) of a second conductivity type that is further disposed on a semiconductor substrate (11) of the first conductivity type; an insulated gate field effect transistor (112) that shares the well region with the photodiode (111), further comprising: a source diffused region (16) of the second conductivity type disposed on a surface of the well region; a drain diffused region (17a) of the second conductivity type disposed on a surface of the semiconductor layer other than the surface of the well region (portion of 17a is formed on the surface of the semiconductor layer 12 other than

the surface of the well region 15); a gate electrode (19) formed above the well region between the drain diffused region (17a) and the source diffused region (16) with a gate insulating film (18) therebetween; a channel region (col. 9, lines 18-20) disposed in the surface of the well region under the gate electrode having an impurity layer of the second conductivity type; and an accumulation region that is heavily doped of the first conductivity type (25), and that is disposed beneath the channel region and adjacent to the source diffused region (16), the accumulation region having an impurity concentration higher than that of the well region (refer to fig. 3) and that accumulates a charge of a given conductivity type generated in response to light incident on the photodiode (col. 9, lines 34-39).

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. References A and B are cited as being related to imaging device. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samuel A Gebremariam whose telephone number is (571) 272-1653. The examiner can normally be reached on 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SAG
February 5, 2005

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